**Lab Assignment- 2**

**Practice Lab**

**Week 2: 11 Aug-18 Aug**

**Lab 2 (hardwired simulation tool)**

1. Design the subtractor circuits with defined bit logic.

2. Design the adder subtractor logic circuits.

3. Design the carry lookup adder, carry select and carry save adder circuits by modifying the ripple carry adder logic given in lab1.

4. See the timing diagram of all four adder circuits and compare which of the adder circuits is best in performance.

5. Design the decoder circuits with defined logic.

6. Design the 4-bit ALU circuits with defined operation logic.